AMD

LDT
(Lightning Data Transport)

CPG Marketing

Technology Evangelism

Jan 24, 2001

LDT Genealogy

AMD

- **LDT was first developed for PC platforms**
  - PCI bandwidth is insufficient for new multimedia devices being integrated into PC core logic
- **LDT has been extended to servers**
  - Coherent LDT is a high speed, low latency interconnect for NUMA architecture multiprocessing systems
- **LDT has found a home in embedded apps**
  - RISC processors for embedded applications are under development by LDT partners
- **A wide range of devices will use LDT**
  - The next spec revision is planned to be less PC specific
  - PC specific information is planned to be put into a PC Design Guide

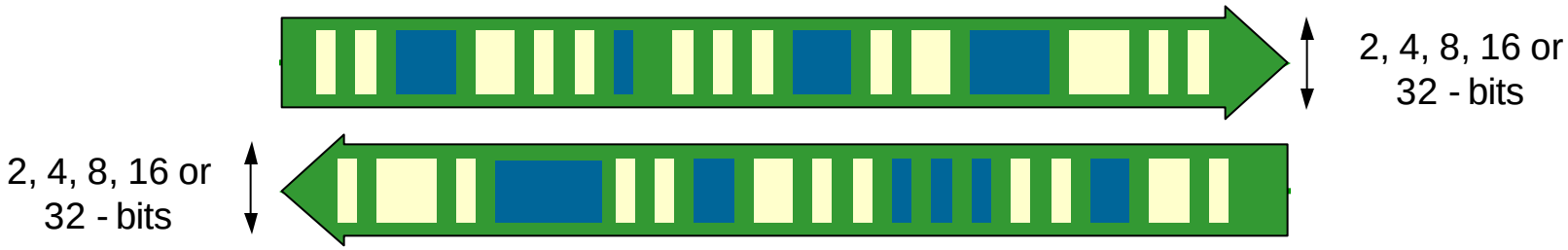
LDT

AMD

- **LDT provides...**
  - a significant increase in I/O bandwidth
  - a universal link that reduces the number of buses within the system
  - support for LDT tunnels that act as I/O building blocks
  - high performance bus for embedded applications
  - highly scalable multiprocessing systems

- **AMD is creating the next generation of PC and embedded platform architecture**
  - For example: AMD PowerNow!™ Technology, LDT, 64-bit x86, DDR memory, and ACR initiatives
  - Offering end users outstanding performance in the industry with LDT

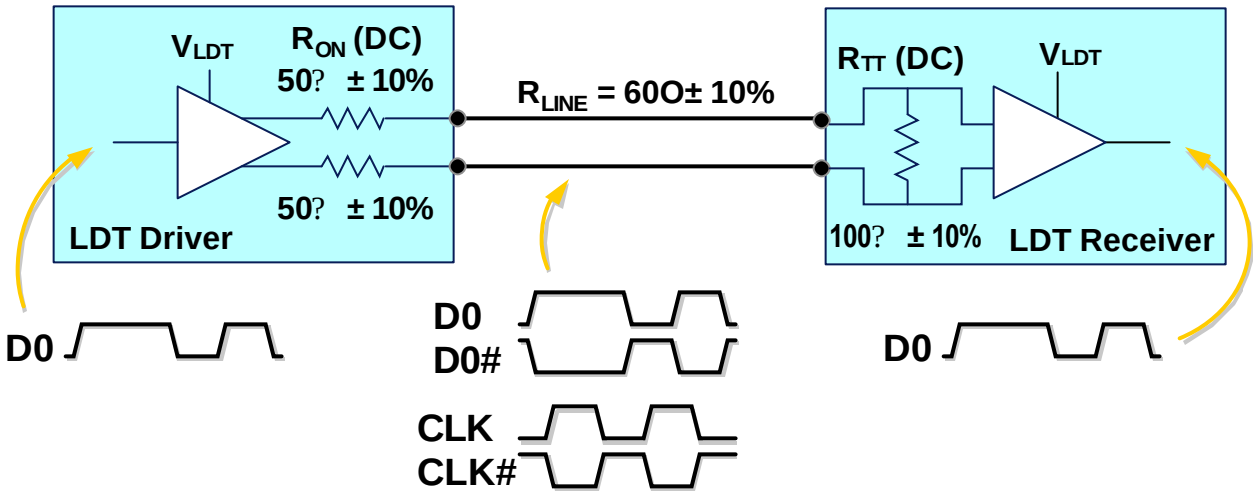
LDT Link Basics



- **LDT connections have two unidirectional point-to-point links**
  - The links can be 2-, 4-, 8-, 16-, or 32-bits wide in each direction
  - LDT I/O has a data rate of 800 Megabits/second per pin-pair (400 MHz clock)
    - **E.g., 8 bits each way gives 800 MB/sec each way; 1.6 GB/sec aggregate bandwidth***
    - **E.g., 4 bits each way gives 400 MB/sec each way; 800 MB/sec aggregate bandwidth***
  - For multiprocessing the CPU-to-CPU link data rate increases to 1.6 Gbits/second
    - **E.g., 16 bits each way gives 3.2 GB/sec each way; 6.4 GB/sec aggregate bandwidth***
- **Packets are multiples of 4-bytes in length**
  - On links < 32-bits, bit times concatenate to achieve the 4-byte granularity
- **Commands, addresses and data use the same bits**
  - Data packets after read responses or writes can be 4- to 64-bytes long

* The sweet spots for LDT configurations

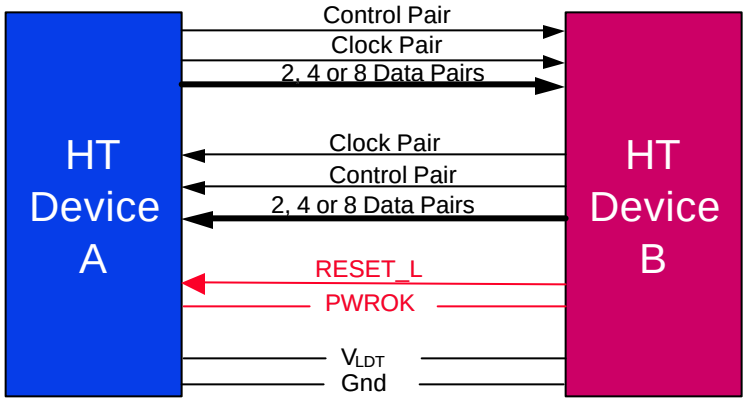
LDT Physical Layer



- **Low voltage, differential signaling**
  - Two pins per bit - pin pairs swing in opposite directions
  - V_{LDT} is 1.2 volts ± 5% resulting in a differential output of 600 $mV_{TYPICAL}$
  - Differential voltage at the receiver inputs can be as low as 200 mV
- **60 ohm differential impedance for low cost PCBs**
  - No special PCB stack-up required
  - Trace lengths up to 24 inches for 800 Mbit/sec operation

LDT Pin Count

- **Additional LDT signals**
  - Power OK (PWROK)
  - Reset LDT (RESET_L)
- **55-pin LDT bus provides 12X the bandwidth of PCI-32/33 with fewer pins**
- **Signal to ground ratio is conservatively 4:1**
- **Optional link power down signals for mobile systems**
  - LDTStop_L
  - DevReq_L
- **Power per pin-pair is nil when in LDT Stop**



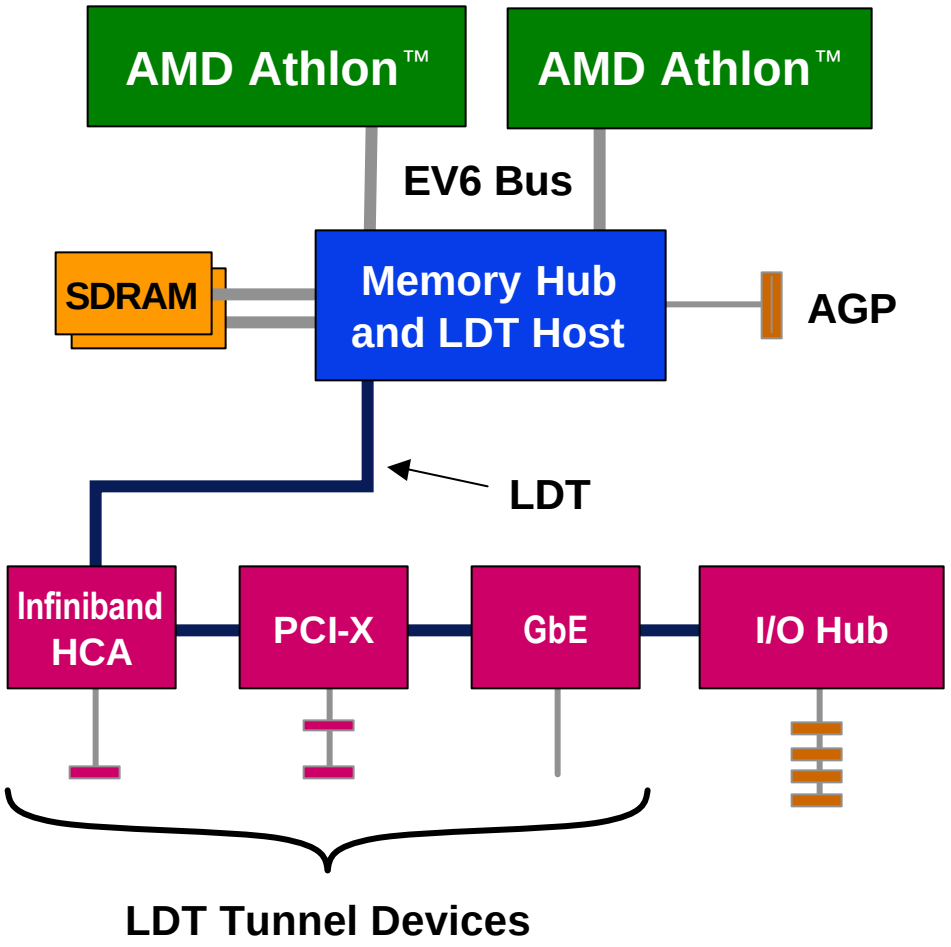
PWROK, RESET_L required for proper reset & init
V_{LDT} routed between devices is required for proper common mode range

Bus Width (Each Way)	2	4	8	16	32
Data Pins (total)	8	16	32	64	128
Clock Pins (total)	4	4	4	8	16
Control Pins (total)	4	4	4	4	4
Subtotal (high speed)	**16**	**24**	**40**	**76**	**148**
VLDT	2	2	3	6	10
GND	4	6	10	19	37
PWROK	1	1	1	1	1
RESET_L	1	1	1	1	1
Total Pins	**24**	**34**	**55**	**103**	**197**

DC Power per Pin-Pair: **4 - 9 mW, 6 $mW_{Typical}$**
Signal to V_{LDT}/Gnd Ratio: **4:1**

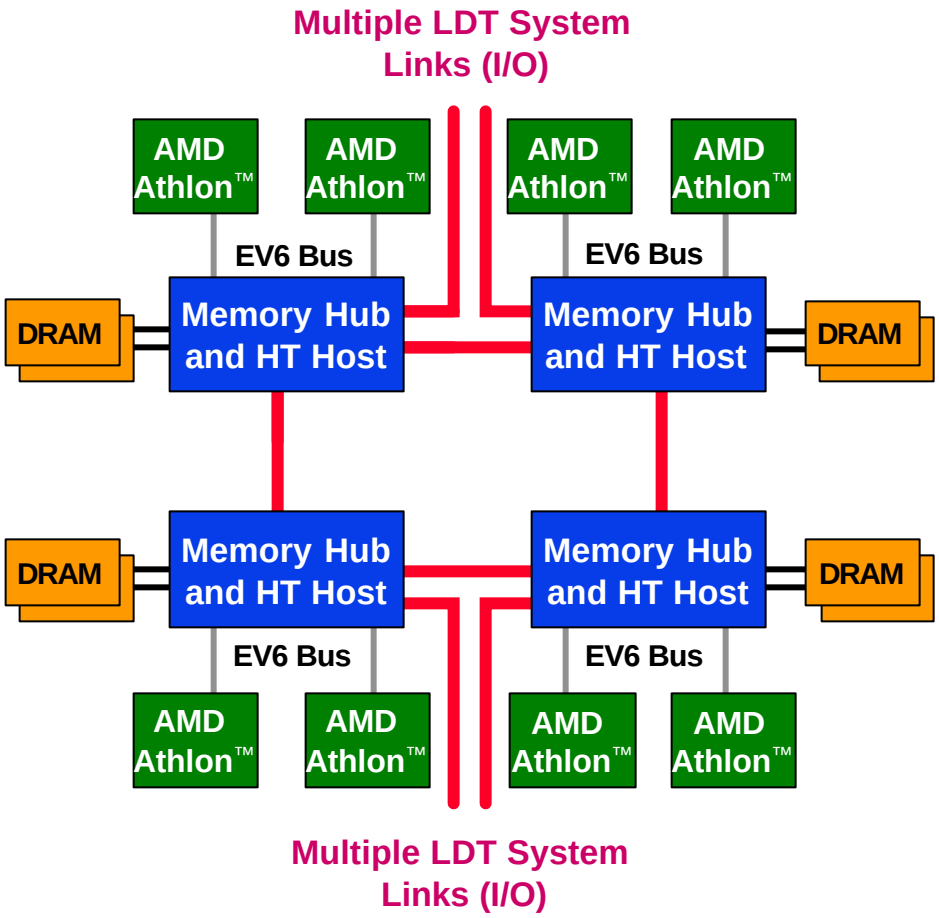
LDT Tunnels

- LDT I/O has ample bandwidth to support daisy chained I/O devices
  - Multiple LDT tunnels can be daisy chained on a single I/O link
  - LDT bridges can be viewed as generic - reusable building blocks for system design
- With LDT tunnels, a basic LDT chipset can be used in server and workstation markets



Coherent LDT Multiprocessing Systems

- **Coherent LDT interprocessor communications for SMP**
  - Coherent LDT handles distant memory access in NUMA* multiprocessor systems
  - Coherent LDT handles probes to maintain system cache coherency
- **Devices have multiple Coherent LDT ports**
  - Coherent LDT is a superset of the LDT I/O protocol, permitting Coherent LDT links to be used for I/O devices
- **Highly scalable SMP systems**
  - Memory capacity scales
  - Memory bandwidth scales
  - I/O capacity scales
  - I/O bandwidth scales



* **N**on-**U**niform **M**emory **A**ccess architecture - each CPU has "local" memory, but can access "distant" memory attached to other CPUs - local memory is faster than shared memory in SMP architecture, hence NUMA machines scale better in systems with large numbers of processors.

LDT Milestones:

AMD

- **First public presentation at Microprocessor Forum 99**
- **Operational Spec version 1.0 finished in May 2000**
  - 1.01C available now (upon signing a license agreement)
- **Electrical Specs nearing completion**
- **LDT presentation with technical information at WinHEC 2000**
  - Great success with about 1500 participants to our session
- **LDT presentation at Platform 2000**
- **1st LDT based chipset announced by NVIDIA**
- **Sibyte (Broadcom) announced their MIPS cpu with LDT**
- **Sandcraft announced their LDT roadmap**
- **NDA signed by 100+ companies, list is growing**
  - about 4-5 new requests are being received each week

LDT Milestones:

- **First licensees. Others to come soon**
  - More than 10 companies signed, others in the pipeline
  - Numerous other companies have expressed the intention to license LDT
- **NDA website established for downloading specs and technical data**
- **LDT white paper available**
- **First FPGA family planned in Q2 2001**
- **Multiple LDT based chipsets for AMD Athlon™ processors in 2001**
  - AMD chipset guys actively working to implement this technology
- **AMD has first silicon samples of a sophisticated south bridge**
  - PCI boards in house with two chips talking to each other using LDT
- **InfiniBand solutions are in design now**
- **LDT-based products are planned from AMD early 2002**
  - Partners plan to have products sooner
- **LDT Consortium planned for 2001**

Call to Action

AMD

- **Gain access to the current LDT I/O specs**
  - Sign specific LDT contributor NDA
    - Specs available with login name and password
    - Access to website with specs, simulation model and names of other LDT NDA-holders
- **To build and market an LDT product**
  - Sign Licensing Contract
    - Gain access to all the related IP
    - Partners may contribute IP, but are not required
- **To build and market LDT technology based PCs**
  - No license necessary if the components are from an AMD licensee
- **For more information, email:**
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  - chris.neuts@amd.com (Sunnyvale, CA)